Digital Design Principles

Half Adder

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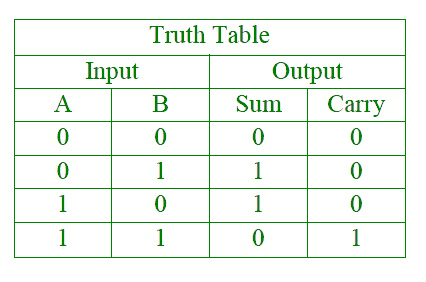
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Objective:

- I use VHDL to implement simple 4-bit half Adder.

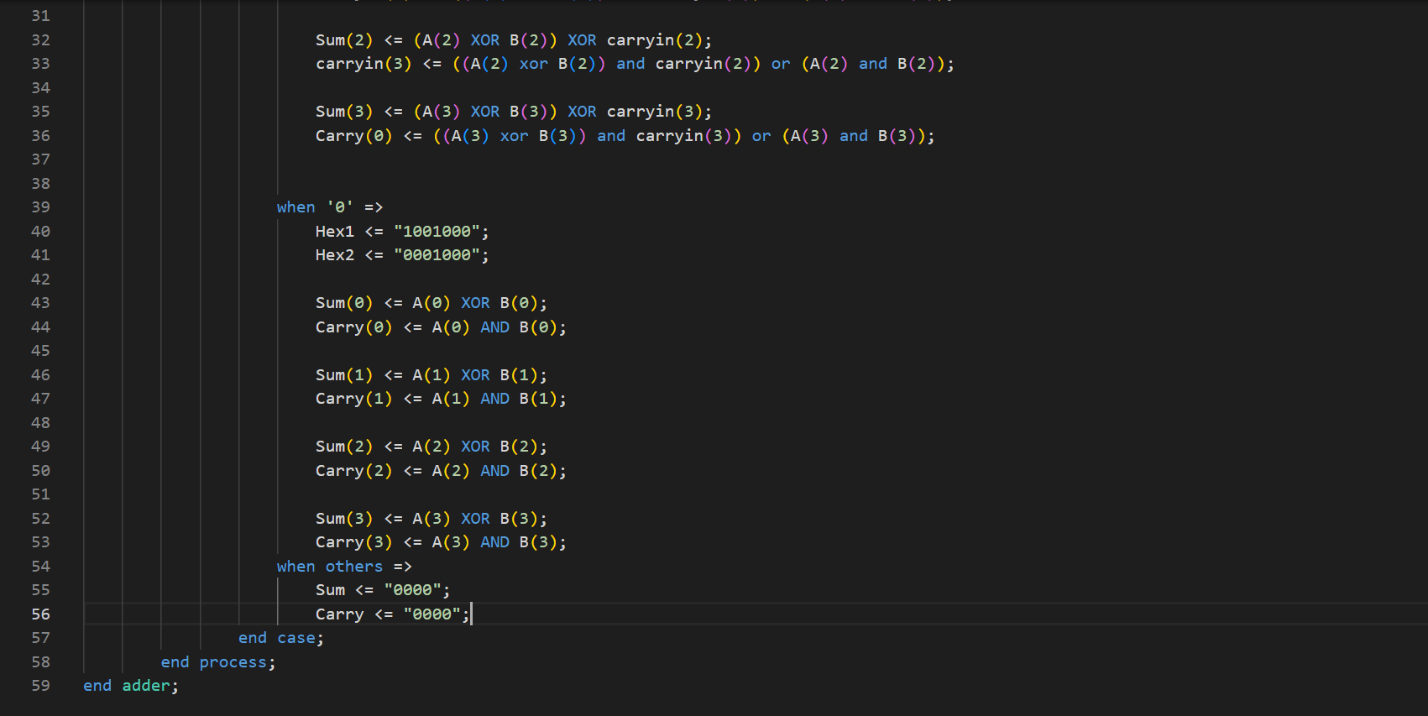
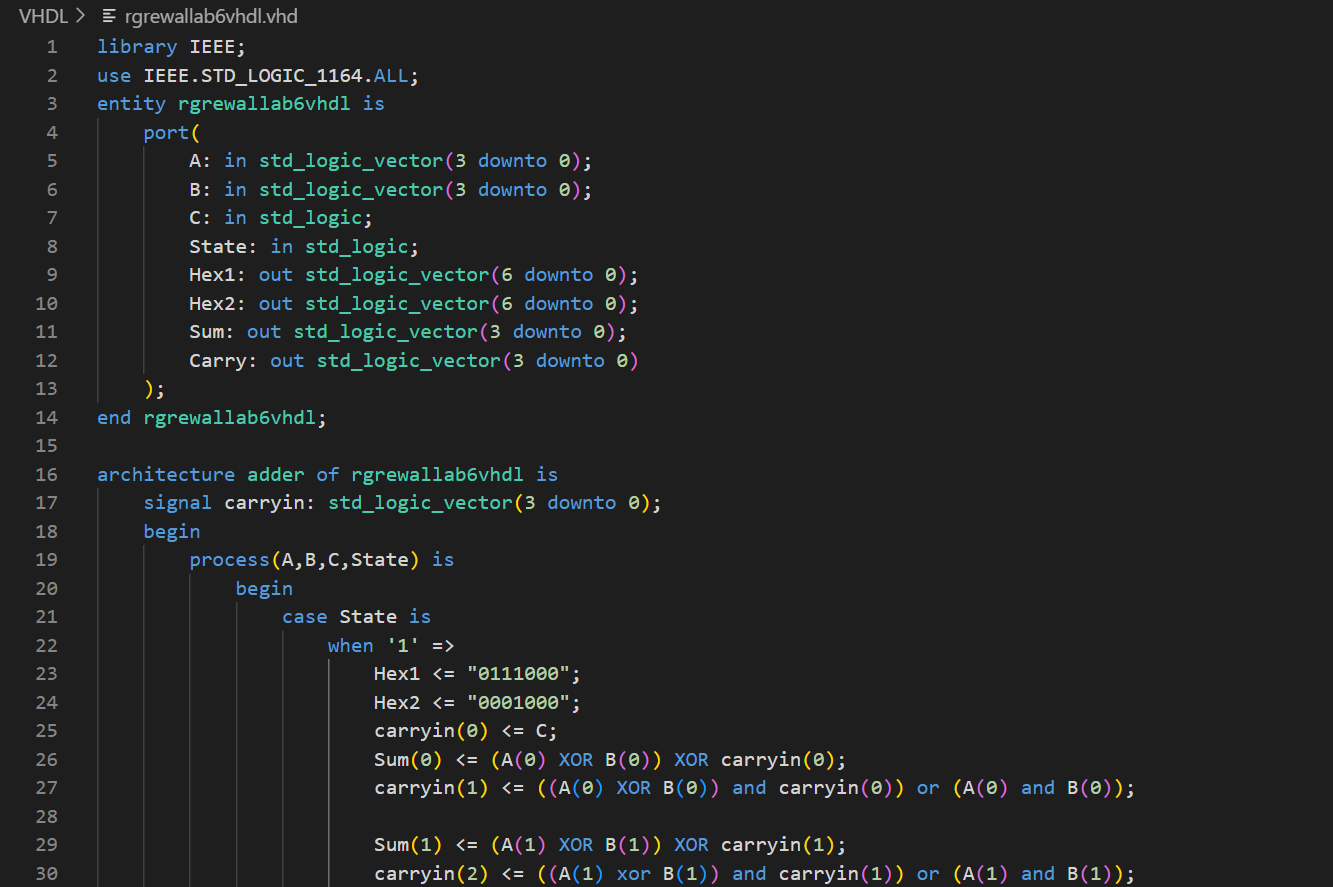
- Set up a project in quartus || targeting your FPGA board.

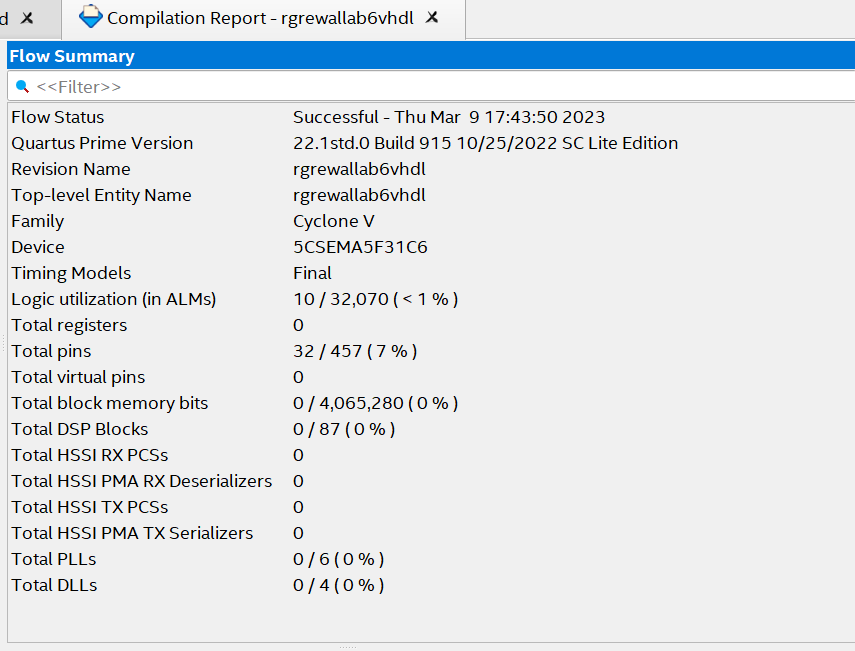
Truth Table:



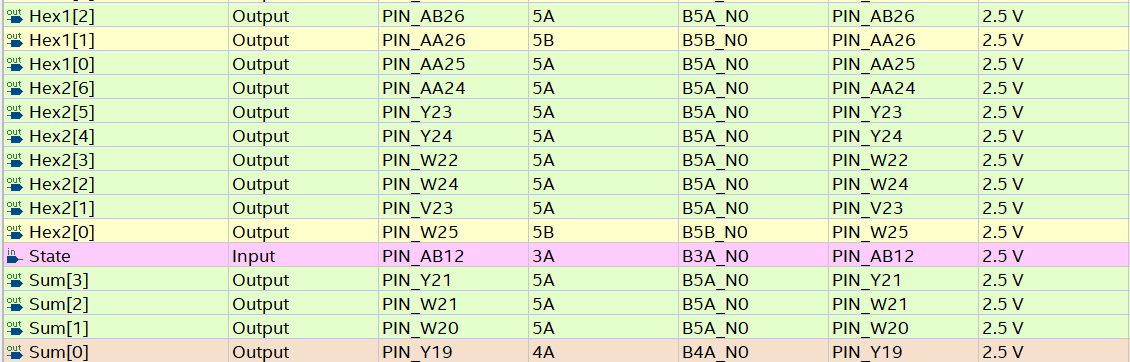
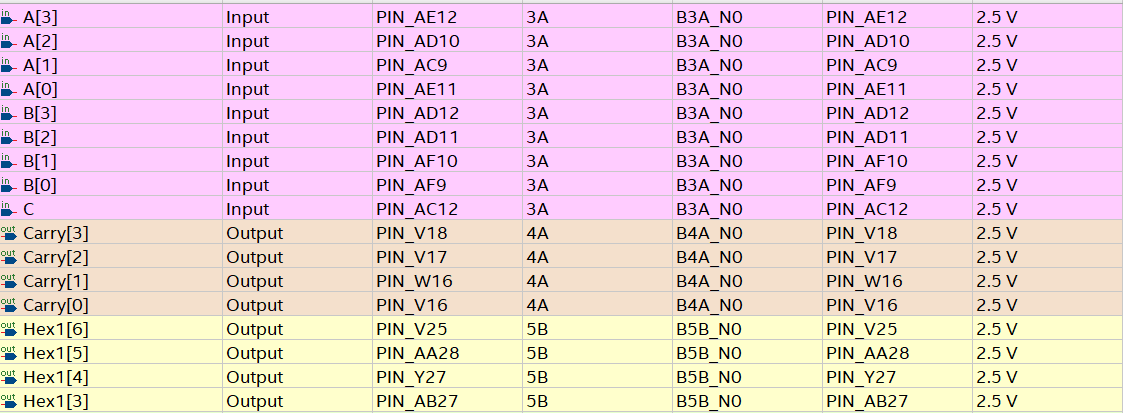
VHDL Introduction:

To make the program in VHDL we will need to initialize the library and entity. Within the entity we will state the vector of 4 switch for a and b. We will also add a switch for carry in and another switch to change from half adder and full adder. For the output we will need a vector to store for the two 7-segment led, and the vector of 4 led for Sum and Carry. Within the architecture of the program, we will have a case where the state switch is checked if it’s on and if it’s on the code of the full adder will run and if it’s not on the code for the half adder will one. If the full adder code is running the first seven segment led will light up F and the second one will light up A. When the half adder is running the first seven segment led will light up H and the second one will light up A. The rest of the program will calculate the Sum and the Carry according to the way the half adder/ Full adder works.

VHDL program screenshot:

VHDL compilation report:

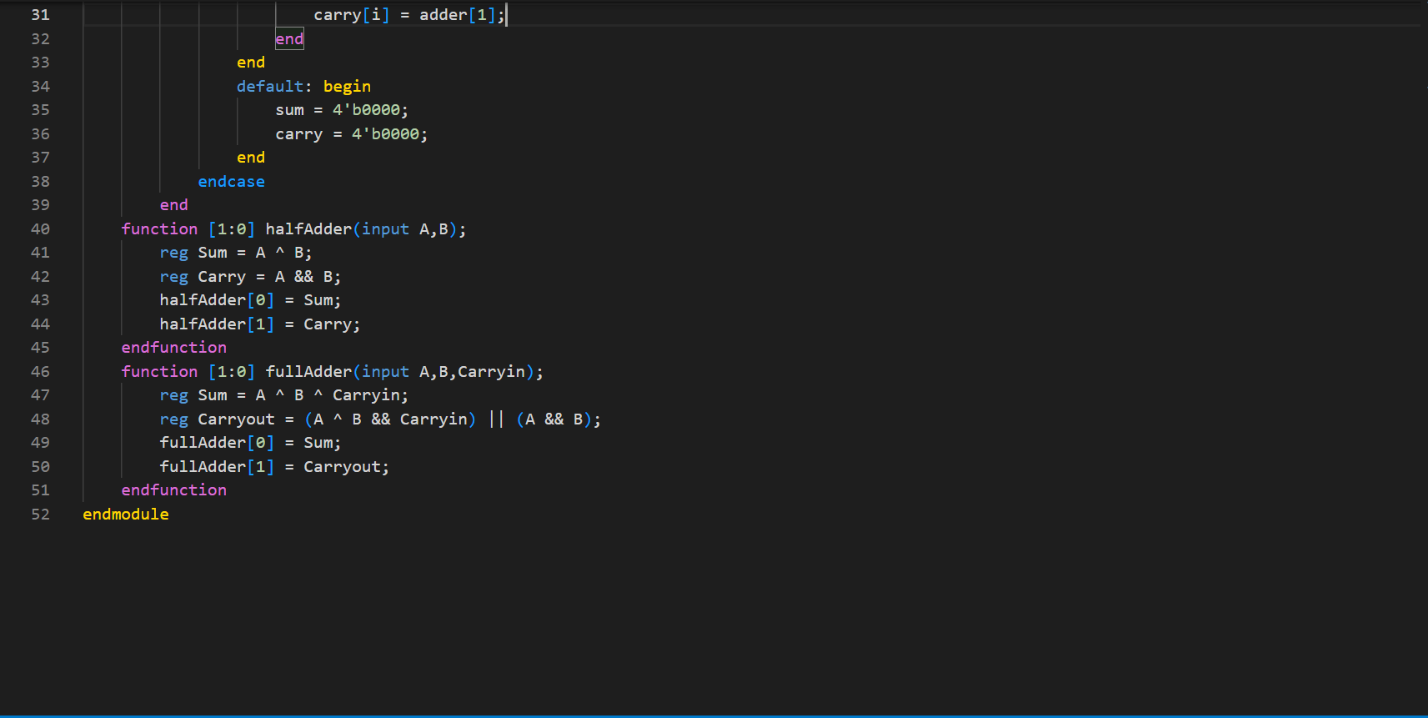
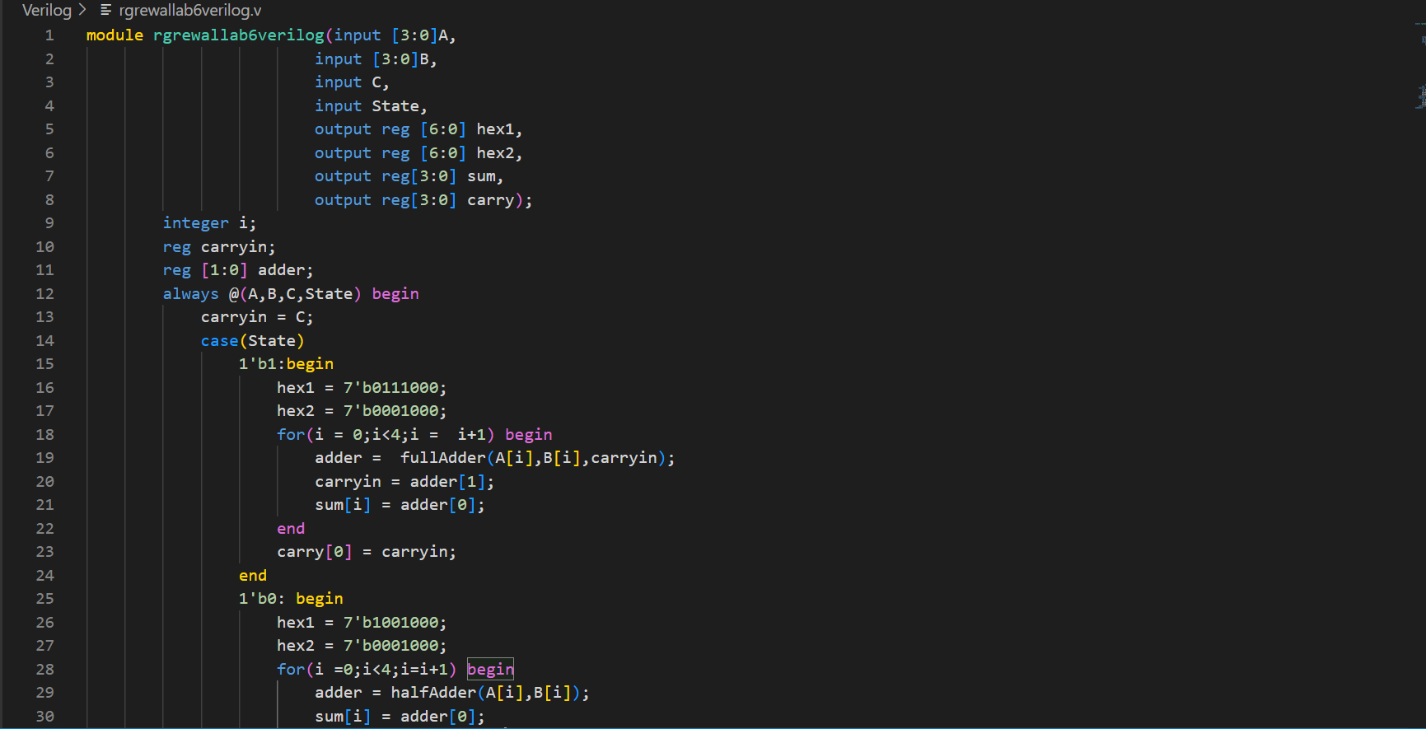
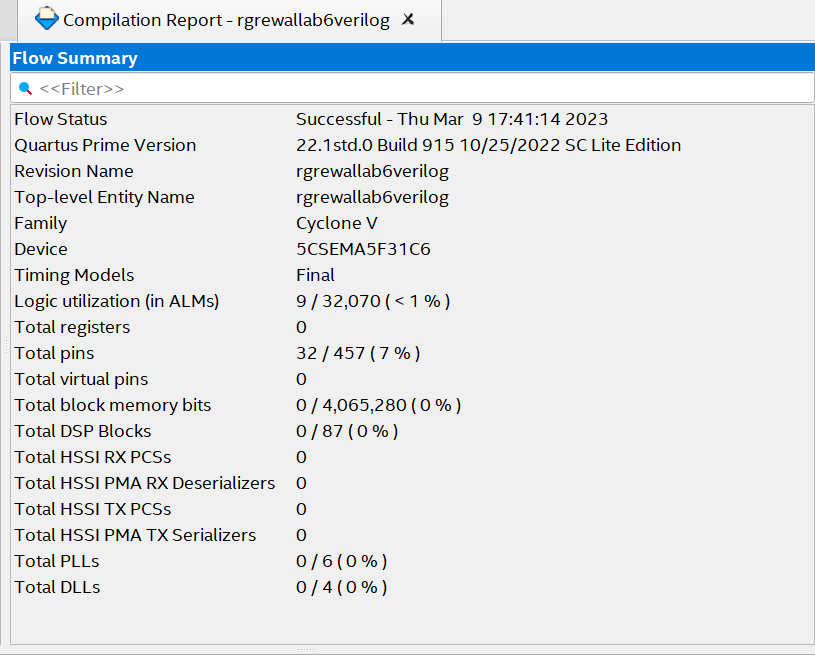
Pin Planner screenshot:

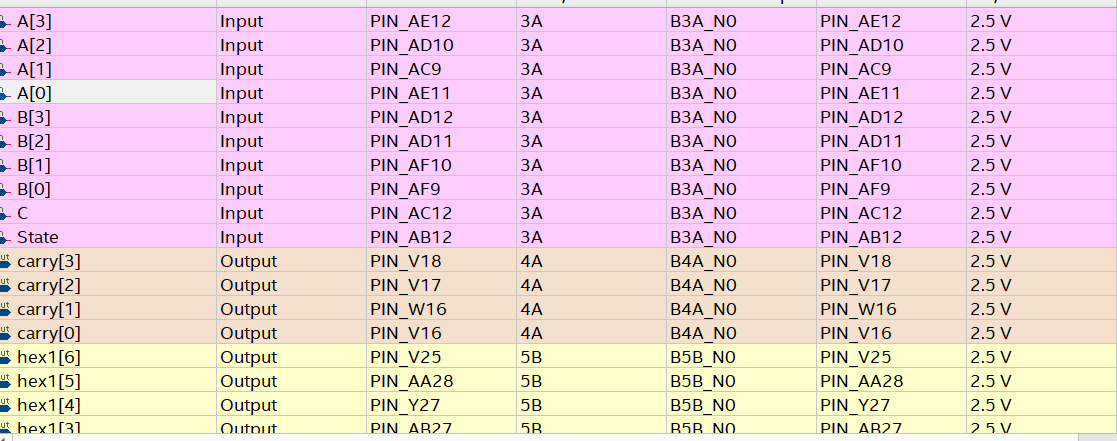


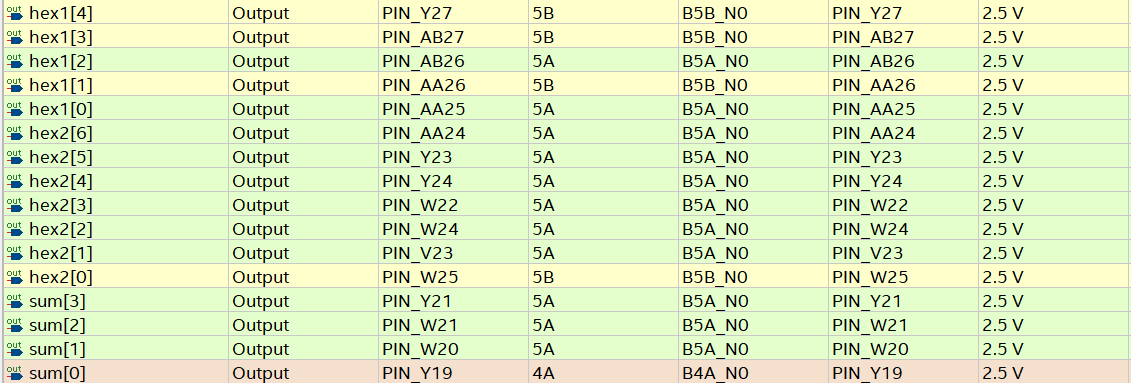
Verilog introduction:

For the program in Verilog we will need to initialize the module with the parameters having we will state the vector of 4 switches for a and b. We will also add a switch for carry in and another switch to change from half adder and full adder. For the output we will need a vector to store for the two 7-segment led, and the vector of 4 led for Sum and Carry. We will have a case where the state switch is checked if it’s on and if it’s on the code of the full adder will run and if it’s not on the code for the half adder will one. If the full adder code is running the first seven segment led will light up F and the second one will light up A. When the half adder is running the first seven segment led will light up H and the second one will light up A. The rest of the program will calculate the Sum and the Carry according to the way the half adder/ Full adder works.

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Verilog program screenshot:Verilog compilation report:

Verilog pin planner screenshot:



Conclusion:

Thus we can conclude that by both the programming languages we will have the led light up according to if the full adder is followed or the half adder is followed. The two seven-segment led will light up according to which state the fpga is in.